96767900

CONTROL DATA CORPORATION

CONTROL DATA®
512- AND 2048-INSTRUCTION MICRO MEMORY
BA209-A, BA210-A, BA210-B

GENERAL DESCRIPTION
INSTALLATION
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released.
(9/76)	
Publication No. 96767900	

REVISION LETTERS I, O, Q AND X ARE NOT USED

Address comments concerning this manual to:

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Publications and Graphics Division
4455 Eastgate Mall
La Jolla, California 92037
or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an ECO or FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
BA209-A	01		
BA210-A	01		
BA210-B	02		

LIST OF EFFECTIVE PAGES

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PREFACE

This manual contains hardware maintenance information prepared to aid maintenance personnel in understanding the circuit operation and application. The content is intended for personnel who have had training and/or experience in the operation and application of similar equipment.

Logic diagrams are not included in this manual. They are incorporated in the field print package that accompanies the system employing random-access memory instruction micro memories.

These boards provide random-access memory storage and retrieval facilities for micro-memory instructions employed in processing systems with micro level programs. The capabilities for each are as follows:

- BA209-A micro memory – 512 x 32 bit instructions
- BA210-A micro memory – 2048 x 32 bit instructions
- BA210-B micro memory – 2048 x 32 bit instructions plus parity check bits

The following documents may be useful to the readers of this manual:

Publication	Publication Number
BA209-A Field Print Package	96751600
BA210-A Field Print Package	96751000
BA210-B Field Print Package	96751100
Basic Micro-Programmable Processor Hardware Maintenance Manual	39451400
Operational Diagnostic System (ODS) Reference Manual	39452100

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FIGURES

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GENERAL

This manual contains maintenance information relative to the 512-instruction micro-memory, the 2048-instruction (2K) micro-memory, and the 2048-instruction (2K) micro-memory with parity printed circuit boards. One to four of any one category (512, 2048, or 2048 with parity) of these boards are employed in the Control Data Corporation 16-bit data word family of CYBER 18 processors. The 2K-instruction micro-memory with parity board is also used in the microprocessor portion of the tape library adaptor (TLA).

DESCRIPTION

PHYSICAL DESCRIPTION

The 2K-instruction micro-memory is a four-layer printed circuit board, and the 512-instruction micro memory and 2K instruction micro-memory with parity boards are three-layer printed circuit boards that measure 11 x 14 inches (see figures 1-1, 1-2, and 1-3). The boards contain capacitors, resistors, and integrated circuits that produce the logical, address, and memory functions. Integrated circuits provide semiconductor memory facilities for two 512/2048 32-bit instructions. One to four of any single type of these micro-memory boards can be installed in any of the four processor slots labeled μMEMORY. The processor backplane may also be custom-wired to double the word length for 32-bit data word machines.

FUNCTIONAL DESCRIPTION

The 512- and 2K-instruction micro-memory boards provide nonvolatile storage of 512 or 2048 32-bit micro instructions for the CDC® CYBER 18-20 and 18-30 processors (figure 1-4). The 2K-instruction micro-memory with parity configuration contains storage for an additional four bits (two bits for each 32-bit instruction) to accommodate the parity bits. All three micro-memory boards are random-access memory (RAM) configurations consisting of read/write memory semiconductor chips that can be loaded externally or under control of the micro program.

The description contained in the following paragraphs pertains to both the 512- and 2K-instruction micro-memory boards. Since both memories function similarly, reference is made to the 2K-instruction micro-memory board only.

The micro memory stores 1024 64-bit words. This storage is subdivided into two 1024 32-bit micro-instruction memories (upper and lower) to provide read/write facilities for 2048 32-bit micro instructions. Each of the 1024 32-bit memories is subdivided into two 1024 16-bit memories, which are referred to as upper and lower. All write data to the micro memory is executed 16 bits at a time and is stored in any of the four 1024 16-bit locations designated by the address code and control logic conditions. Read outputs can be in the form of instructions or operands. These instructions and operands contain 32 bits composed of 16 bits from the upper 1024 x 32-bit memory, to provide the instruction's upper 16 bits (00 through 15) and 16 bits from the lower 1024 x 32-bit memory, to provide the instruction's lower 16 bits (16 through 31). When the write enable signal is low, the data/instruction is written to the upper or lower 1024 x 16-bit locations of the upper or lower 1024 x 32-bit memories designated by the control logic (upper enable and lower enable). When the write enable signal is high, the data/instruction is read from the addressed locations. Then the retrieved 32 bits are gated by the enable B control logic signal to the processor transform board (16 bits from the upper to provide the 00 through 15 bits, and 16 bits from the lower to provide the 16 through 31 bits).

In the CYBER 18 processors, up to four instruction micro-memory boards may be employed. Each board contains four switches that are set to designate the micro-memory page assignment. This switch code (A) and the processor designation code (B) are sensed by the designation comparator. When the two codes coincide (A code = B code), the designated micro-memory board is enabled. Enabling any one of the micro-memory boards disables all associated micro-memory (page) boards.

When enabled, the selected micro-memory boards' selection detectors enable the upper or lower 1024 x 32-bit memory that is to store (write) or release (read) the data/instruction bits. The bits are stored in or released from the locations designated by the address bits. Released (read) bits are applied to the associated A and B inputs of the upper and lower selectors. All 32 bits from the addressed locations of the enabled (upper or lower) 1024 x 32-bit memories are applied to the selectors. The state of the enable B signal determines which bits (A or B) are placed on the output lines. When the enable B state is low the A inputs are selected, and when the enable B state is high the B inputs are selected. The selected output data/instruction bits are coupled to the transform, control 1, and control 2.

When either of the 2K-instruction micro-memory boards is employed in a 32-bit data processor, 32 data bits are coupled via the read gates to the processor. This requires custom wiring of the backplane connectors.

The 2K-instruction micro-memory with parity boards add a parity check bit with each 16 bits stored or released. Therefore, an instruction consists of 34 bits and an operand consists of 17 bits.

The 512-instruction micro-memory boards do not contain output selection multiplexers. Therefore, selection of the instruction bits and operand bits to be coupled to the processor is determined by chip enable signals.

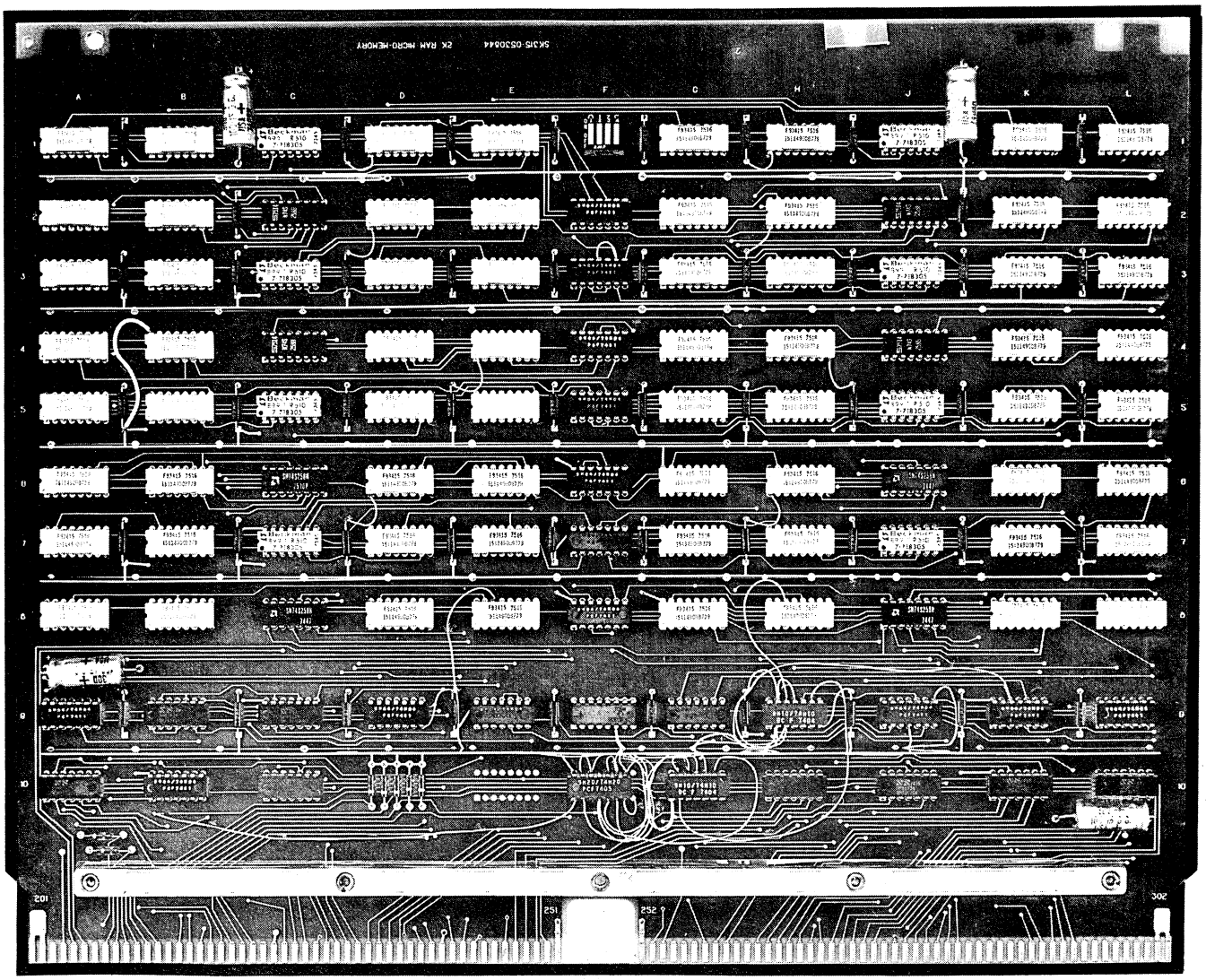


Figure 1-1. 2K-Instruction Micro-Memory Board

REFERENCE DATA

MEMORY CAPACITY

2K-instruction micro memory: 2048 micro instructions†

2K-instruction micro memory with parity: 2048 micro instructions plus 4 parity bits†

512-instruction micro memory: 512 micro instructions†

†One micro instruction equals 32 bits.

POWER REQUIREMENTS

2K-instruction micro-memory board: +4.75 to +5.25 vdc at approximately 7.0 amperes. Average power consumption is 35 watts.

512-instruction micro-memory board: +4.75 to 5.25 vdc at approximately 5.3 amperes. Average power consumption is 28 watts.

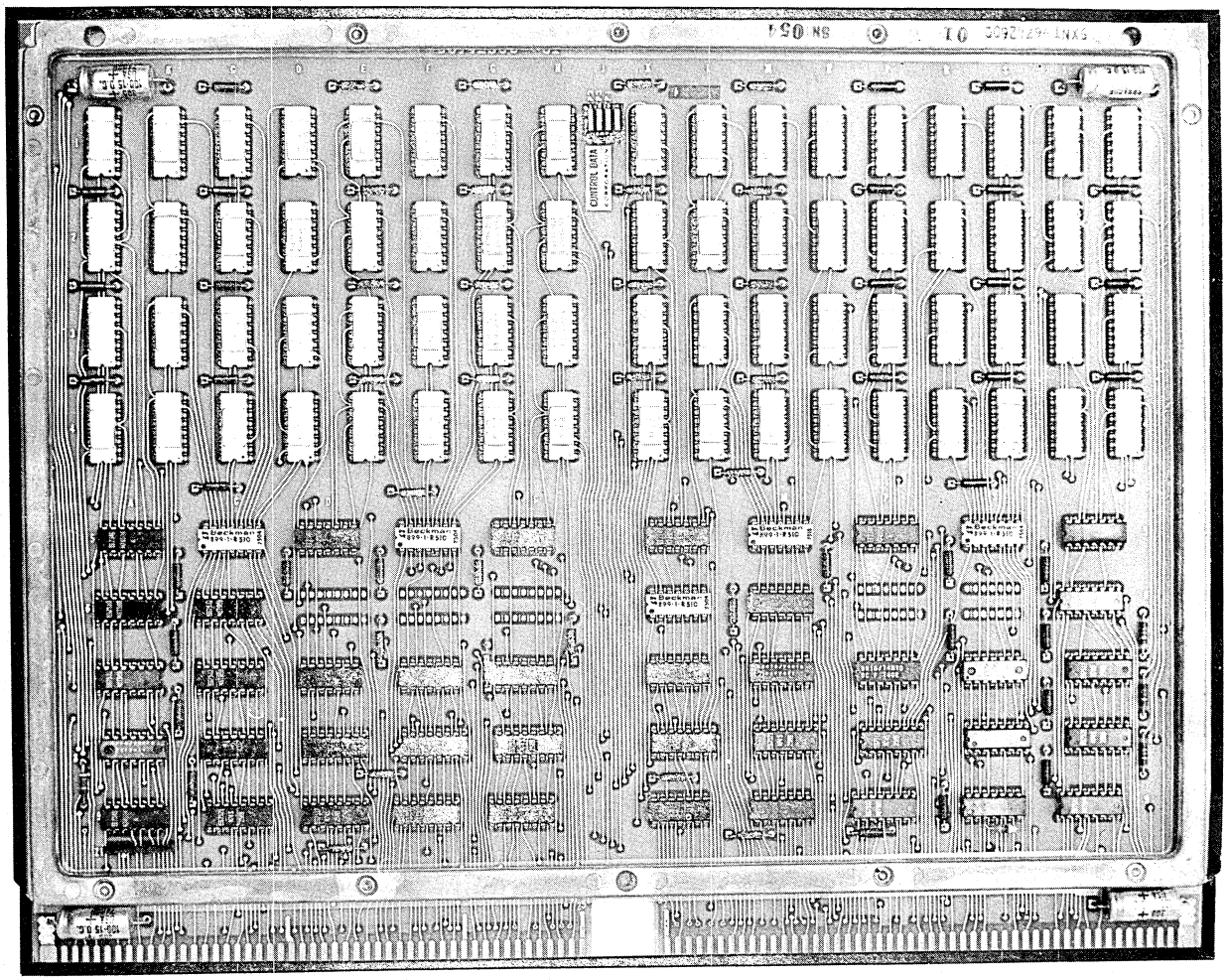


Figure 1-2. 2K-Instruction Micro-Memory Board With Parity

MICRO-MEMORY TIME CHARACTERISTICS

Basic instruction cycle time: 168 nanoseconds

Access time: 70 nanoseconds

Read/write operand time: 504 nanoseconds

OPERATING ENVIRONMENT

Temperature: 40° to 120° F (4.4° to 48.9° C)

Altitude: Sea level to 10,000 feet (300 meters)

Humidity: 10 to 90 percent relative at 104° F (40° C) (non-condensing)

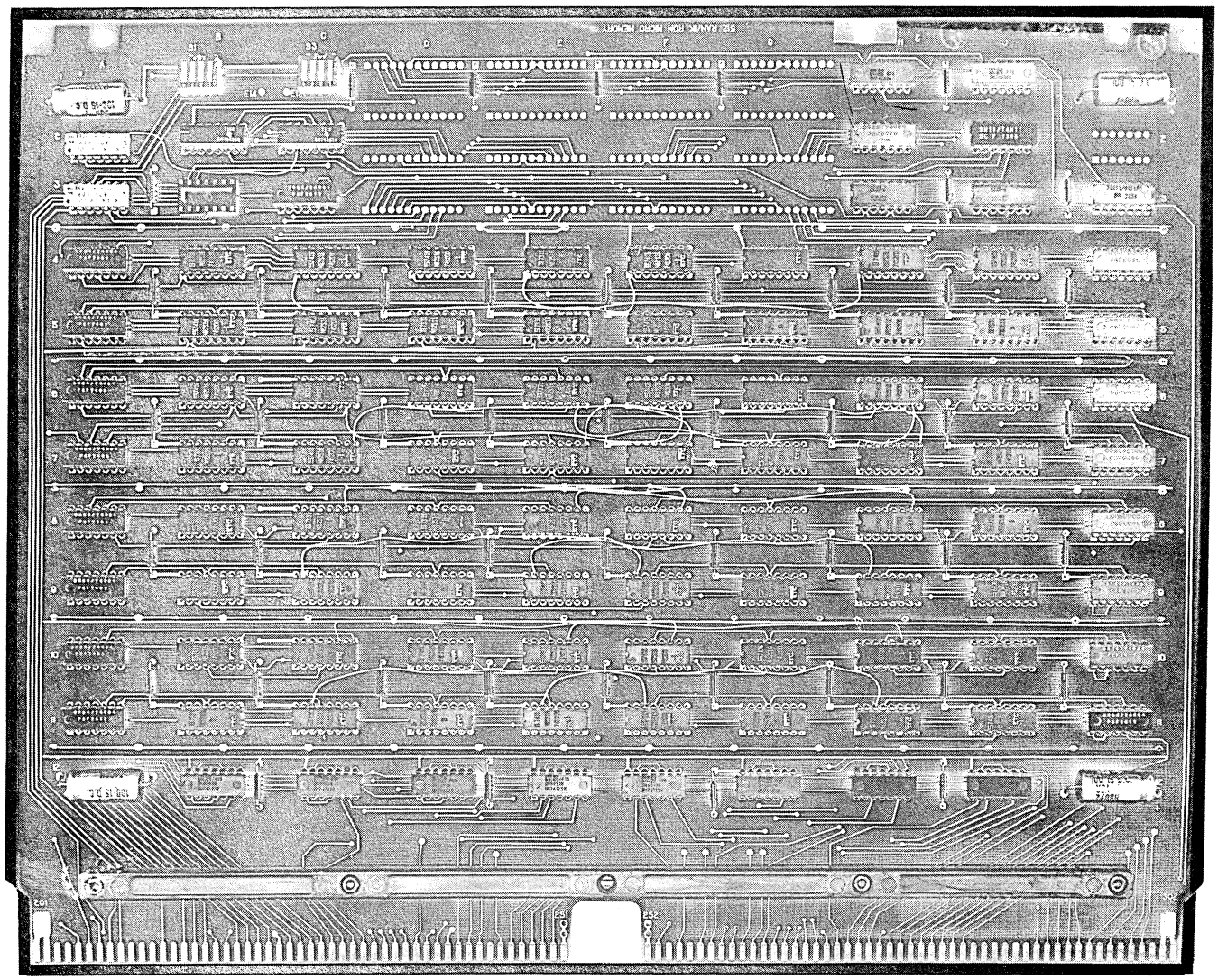


Figure 1-3. 512-Instruction Micro-Memory Board

DATA FORMAT

Parallel 16 bit in

Parallel 16 and 32 bit out

SIZE

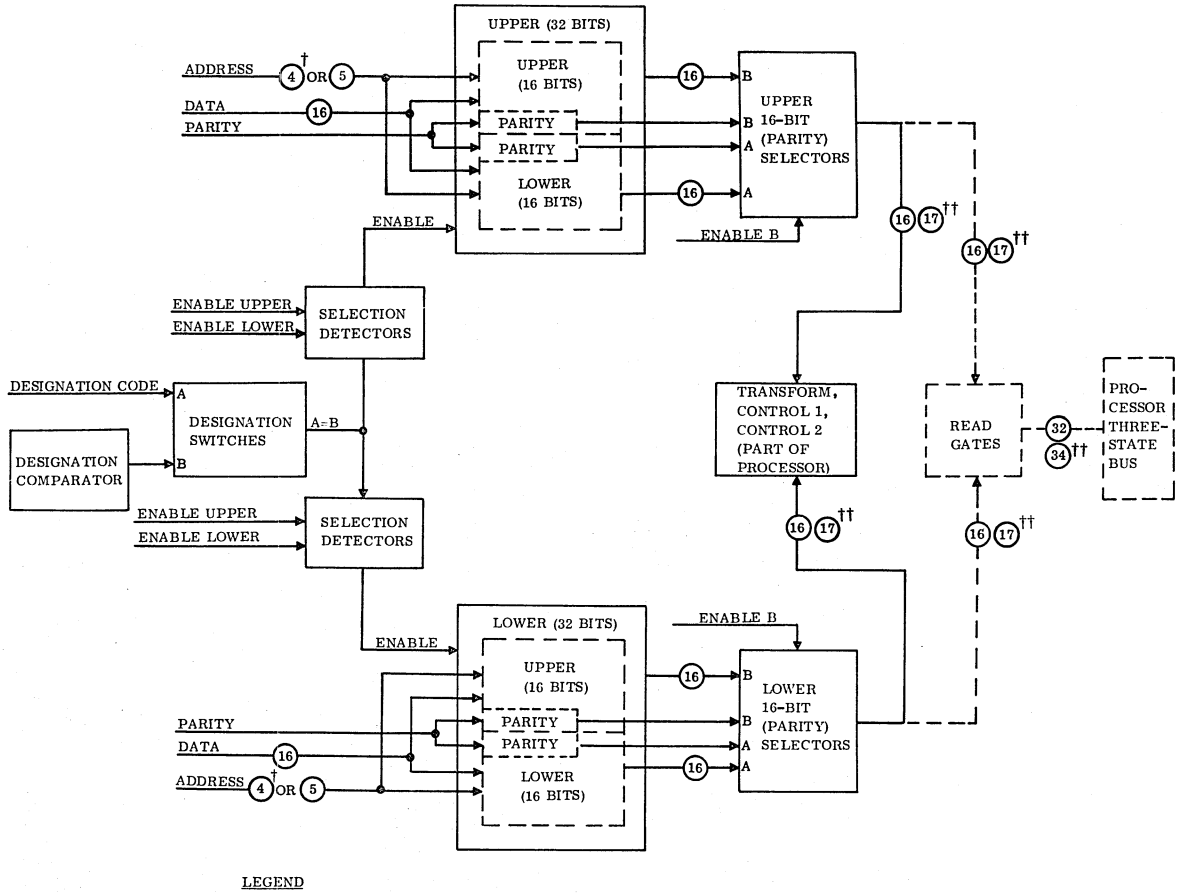
Height: 14 inches

Width: 11 inches

LOGIC (TTL)

Logical zero (low) 0.0 to 0.8 vdc

Logical one (high) 2.0 to 5.25 vdc



LEGEND

(2) INDICATES NUMBER OF LINES

---INDICATES ADDITIONAL OUTPUT FOR 32-BIT DATA PROCESSORS

† APPLICABLE TO 512-INSTRUCTION MICRO MEMORY

†† APPLICABLE WHEN PARITY CHECK IS EMPLOYED

0260

Figure 1-4. RAM Micro Memory Block Diagram

There is no operation or programming information associated with the operation of any of the micro-memory boards.

The micro-memory printed circuit board plugs into the processor chassis in any one of the slots marked μMEMORY (slots S, T, U, or V). Before a board is inserted, the page switches (F1) must be set to designate the board's page assignment (0 through 15). (Page/switch selection is given in section 4.) Once the switches are set, they designate the specific pages of micro memory assigned to the board, and the board cannot be changed to another location without first resetting these switches.

Processors that process 32-bit operands utilize full 32-bit input. Therefore, the S200 through S215 lines load the upper 32 memory chips and the *S200 through *S215 lines load the lower 32 memory chips. The *S200 through *S215 lines require separate connection at the backplane. If data is to be coupled to the processor three-state bus via bus lines 00 through 31, the *MM00 through *MM31 lines must be connected at the backplane terminals to the corresponding MM00 through MM31 lines.

This section contains the external and internal interface signal diagrams and tables. The external output/input diagrams depict the signal source and termination, and table 4-1 defines the write, read, and control signals that enter and leave the RAM micro memory. Detailed descriptions of the internal micro-memory functions are illustrated in block diagram form. The numbers in the upper right-hand corner of the blocks indicate the field print package pages that contain the logic that the block represents.

EXTERNAL INTERFACE

Table 4-1 tabulates the data, address, and control signals applicable to the RAM micro memory and provides a functional description for each. A graphic representation of this information is included in figures 5-1 and 5-2. The logic diagrams in the field print package contain diagonal (xxxx/) and bar (xxxxx) symbols to indicate active low (not) conditions of signals. The diagonal is used to designate the low condition of micro-memory external signals. The bar is used to designate the low condition of the micro-memory internal signals. (Example: MA00/ through MA07/ and S200/ through S215/ are external signals; $\overline{S200}$ through $\overline{S215}$ and $\overline{ENMML}$ are internal signals.) Some signals are preceded by an asterisk (*). The asterisk applied to input signals designates signals applicable to the development of the lower 16 bits (16 through 31) for a 32-bit data word system, as in the case of *S200 through *S215; otherwise, these signals are paralleled with the S200 through S215 bit lines. The asterisk applied to output signals *MM00 through *MM31 indicates signals that are applicable to 32-bit word processors. These signals are coupled via the bus lines to the central processing unit.

MICRO MEMORY

The micro memory has three configurations: 2K, 2K with parity, and 512 instructions. The 2K-instruction micro-memory configuration provides storage for 2048 x 32-bit data/instructions; the 2K-instruction micro-memory with parity configuration provides storage for 2048 x 36-bit (including four parity bits) data/instructions; and the 512-instruction micro-memory configuration provides storage for 512 x 32-bit data/instructions. Data is stored 16 bits at a time into one of four 1024 x 16-bit minor (upper or lower) memories contained within the 1024 x 32-bit major (upper or lower) memories. Retrieved data/instructions (32 bits) are composed of 16 bits from either the upper or lower minor memory of the upper major memory and 16 bits from the respective minor memory of the lower major memory.

2K-INSTRUCTION MICRO MEMORY WITH/WITHOUT PARITY

NOTE

In the following paragraphs, references to the 2K-instruction micro-memory with parity board are enclosed in parentheses ( ). When reference designations do not differ, no parentheses are used.

The 2K-instruction micro-memory board stores a total of 1024 64-bit words (1024 64-bit words plus four parity bits in 2K-instruction micro-memory with parity board) in two 32 (34)-bit major memories, upper and lower. See figure 4-1 for a functional block diagram of the 2K-instruction micro-memory board. Each of these upper and lower 32 (34)-bit major memories contains two 16 (17)-bit minor memories, also designated upper and lower. Therefore, signal mnemonics contain references to the upper and lower minor memories of the upper major memory; and likewise for the lower major memory (upper of the lower and lower of the lower). Mnemonics used to designate the enable signals for these memory locations are arranged to indicate the upper of upper, lower of upper, upper of lower, and lower of lower destinations for the input data. (For example, the mnemonic MMWU16-U designates a write enable for the upper 16-bit minor memory of the upper 32-bit major memory, and likewise for the MMWL16-U, MMWU16-L, and MMWL16-L.) Each major memory consists of 32 (34) 1024-bit write/read integrated circuit chips. Data (parity) bits are stored in memory cells designated by the write signal, the location enables, and the address bits. Data (parity) bits are retrieved from memory cells designated by the address bits, write enable low, and the selection multiplexer enable signals. Stored data (parity) bits are the complement of the input data, received from the processor. Retrieved data (parity) bits, at the selection multiplexer output, are the complement of the stored data bits. The output data/instruction is composed of 16 (17) bits from the upper major memory and 16 (17) bits from the lower major memory. This data/instruction output from the selection multiplexers is coupled to the transform, control 1, and control 2 facilities of the processor.

TABLE 4-1. EXTERNAL INPUT/OUTPUT SIGNAL APPLICATION

Signal	Source	Application
BUS00-BUS15 *BUS00-*BUS15	Micro memory	Memory data applied to the central processing unit three-state bus
CONENUM-1,2,x	Micro memory	Constant enable of micro memory
DISABLE x	Micro memory	Micro-memory disable of the associated undesignated micro-memory boards
ENMM	Control 1	Enable micro-memory read or write operation
ENMML	Control 2	Enable micro-memory lower instruction
ENMMU	Control 2	Enable micro-memory upper instruction
MA00-MA07	Control 2	Memory address bits to designate the location in memory where the data bits are to be stored
MM00-MM31	Micro memory	Micro-memory output data bits to transform
*MM00-*MM31	Micro memory	Micro-memory output data bits transferred to central processing unit three-state bus (applicable to 32-bit word configurations)
MMWL16	Control 1	Micro-memory write lower 16 bits, writes data instruction bits into the lower memory banks (16 through 31)
MMWU16	Control 1	Micro-memory write upper 16 bits, writes data instruction bits into the upper memory banks (0 through 15)
PG0-PG3	Control 2	Page address bits to select a respective board; and in 2K boards provide address designation along with memory address signals
SELGETMAK	Control 1	Micro level signal that inhibits the micro-memory output when GETMAK is initiated
S200-S215 *S200-*S215	ALU(S2)	Data bits from selector 2 of ALU to be stored in micro-memory upper and lower banks
TEST POINT1-3	2K-instruction micro memory	Provides facilities for testing switch conditions
XTPAGE 0	Transform	Transform page 0 disable of micro memory, when transform micro-memory feature is selected
ENMML/ENMMU-A ENMML/ENMMU-B ENMML/ENMMU-C (512 RAM only)	512-instruction micro memory	Enable micro-memory lower/enable, micro-memory upper A, B, C; used to produce the micro-memory enable logic for enabling the minor memory banks
ENMMLB (512 RAM only)	Micro memory	Enables read gates of the lower 16 bits (16 through 31) of word applied to the bus line output
ENMMUB (512 RAM only)	Micro memory	Enables read gates of the upper 16 bits (00 through 15) of word applied to the bus line output
MML-PAR (2K with parity only)	Micro memory	Output parity bit associated with lower 16 bits (16 through 31)

TABLE 4-1. EXTERNAL INPUT/OUTPUT SIGNAL APPLICATION (Continued)

Signal	Source	Application
MMU-PAR (2K with parity only)	Micro memory	Output parity bit associated with upper 16 bits (00 through 15)
S2PAR		Input parity bit associated with the upper and lower 16 bits of the upper 32-bit memory bank
S2PAR*		Input parity bit associated with the upper and lower 16 bits of the upper 32-bit memory bank

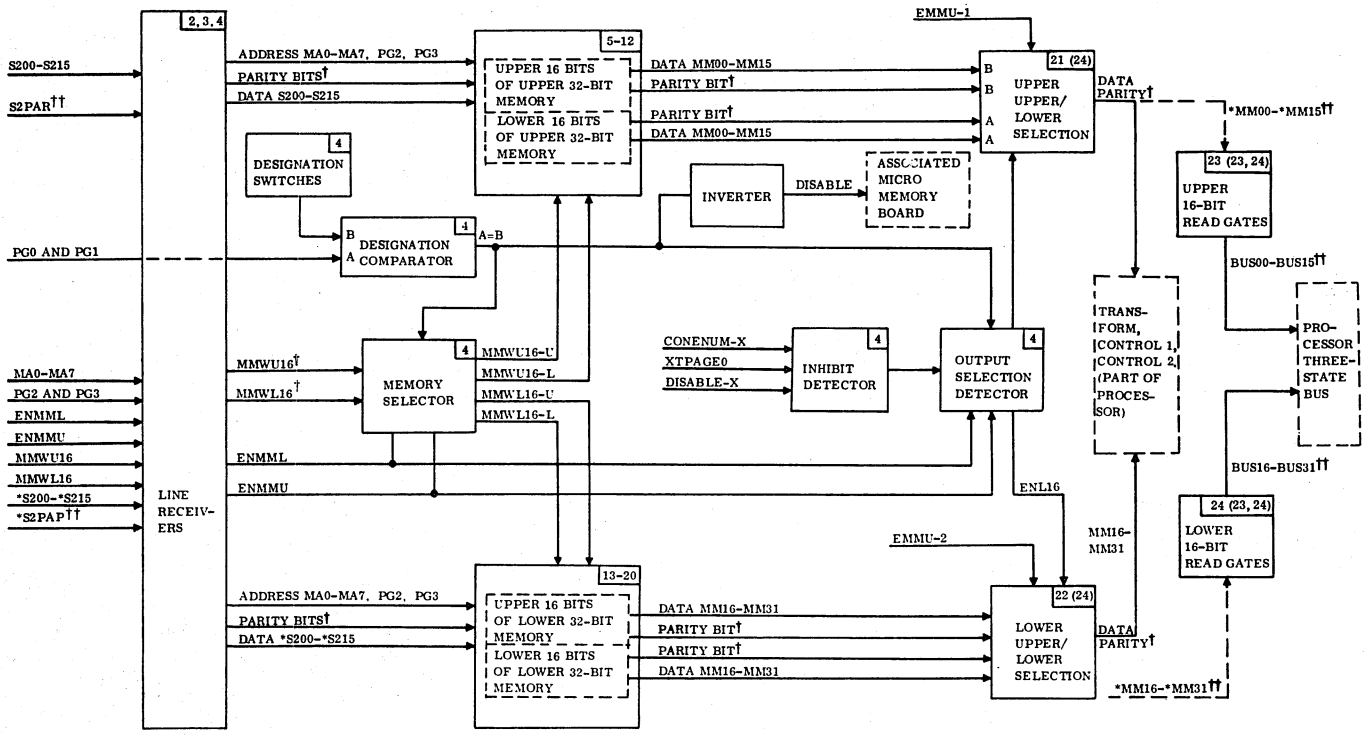


Figure 4-1. 2K Micro Memory Functional Block Diagram

Selection

The designation switch F1, is set at the time of installation to indicate the assigned micro-memory page of each individual board: pages 0 through 3, 4 through 7, 8 through 11, and 12 through 15. Refer to table 4-2 for switch settings. The switch code is applied to the B input of the comparator F9 (F10). When the page bits (PG0 and PG1) code applied to the A input equals the B code, the output at A = B goes high. This high enables the memory selector AND gates G10 and H9 (G11 and H10), the selection detector AND gates F10 and G10 (E11 and G11), and the disable inverter, F8.

TABLE 4-2. PAGE SWITCH SELECTION

S0	S1	S2	S3	RAM Board Selected
OFF	OFF	OFF	Not used	Pages 0 through 3
OFF	ON	OFF	Not used	Pages 4 through 7
ON	OFF	OFF	Not used	Pages 8 through 11
ON	ON	OFF	Not used	Pages 12 through 15

Write

The memory selector AND gates decode the write memory selection inputs MMWL16, MMWU16, ENMM, ENMML, and ENMMU to determine which memory bank stores the input data (parity) bits. The state of these input signals (table 4-3) causes one of the AND gate outputs, MMWL16-U, MMWL16-L, MMWU16-U, or MMWU16-L, to go low, and enables storage of data (parity) by the enabled memory chips. Refer to table 4-4 for mnemonic descriptions.

When logic states A = B high, MMWU16 low, and ENMMU high exist, they produce a low state of MMWU16-U at output pin 12 of AND gate H9 (H10). This low state is applied to the write enable input, pin 15, of memory chips B1 through B8 and H1 through H8 (B1 through B8 and H1 through H9) to select the write (store) operation. With the write function selected, the data (parity) on lines S200 through S215 (S2PAR) is stored in the memory data (parity) location designated by the address bits MA0 through MA7, PG2, and PG3. When logic states A = B high, MMWL16 low, and ENMMU high exist, they produce a low state of MMWU16-L at output pin 12 of AND gate G10 (G11). This low state is applied to the write enable inputs of memory chips A1 through A8 and G1 through G8 (A1 through A8 and G1 through G9) to select the write (store) operation. With the write function selected, the data (parity) on lines S200 through S215 (S2PAR) is stored in the memory data (parity) locations designated by the address bits. Data (parity) storage into the lower 32 (34)-bit memory bank is accomplished in the same manner as the upper memory banks, through utilization of AND gates H9 (H10) associated with write control signals MMWU16-L and MMWL16-L. The lower 32 (34)-bit memory banks store the *S200 through *S215 data (S2PAR*) bits.

Read

The memory banks are always enabled for data retrieval (read) since the write enable input at the memory chip is high. An individual printed circuit board is enabled for reading when the comparator's output, A = B, goes high. This enables the output selection detector AND gates F10, G10 (E11, G11) and initiates the disable output from

TABLE 4-3. DATA STORAGE

Input Signals					Write Enable	Memory	Data (Parity)
ENMMU	ENMML	MMWU16	MMWL16	A = B	Signal	Chips	Stored
H		L		H	MMWU16-U	B1 through B8 H1 through H8 (B1 through B8) (H1 through H9)	S200 through S215 S200 through S215 + parity
H			L	H	MMWL16-U	E1 through E8 L1 through L8 (E1 through E8) (L1 through L9)	*S200 through *S215 *S200 through *S215 + parity
	H	L		H	MMWU16-L	A1 through A8 G1 through G8 (A1 through A8) (G1 through G9)	S200 through S215 S200 through S215 + parity
	H		L	H	MMWL16-L	D1 through D8 K1 through K8 (D1 through D8) (K1 through K9)	*S200 through *S215 *200 through *215 + parity

TABLE 4-4. INTERNAL SIGNAL DESCRIPTION

Mnemonic	Description	Function
ENL16 ENU16	Enable lower 16 Enable upper 16	Enable/inhibit lower and upper read selection multiplexers
ENMMU-1 ENMMU-2	Enable micro memory Upper 1 and 2 (A and B)	Selection of read selection multiplexers A and B outputs
MM00-A through MM31-A MM00-B through MM31-B	Micro-memory read bits 00 through 31 (00=LSB, 31=MSB)	Read data bits transferred from memory cells to read selection multiplexers
MMWL16-L	Micro-memory write lower 16 lower	Enable signals for selecting upper and lower 16-bit storage cells of the upper and lower 32-bit banks
MMWL16-U	Micro-memory write lower 16 upper	
MMWU16-L	Micro-memory write upper 16 lower	
MMWU16-U	Micro-memory write upper 16 upper	
MML16PAR-A	Micro-memory lower 16 parity-A	Parity bits associated with the read data bits transferred to the read selection multiplexers
MML16PAR-B	Micro-memory lower 16 parity-B	
MMU16PAR-A	Micro-memory upper 16 parity-A	
MMU16PAR-B	Micro-memory upper 16 parity-B	
MA0 through MA7 -2, -3, -4, and -5	Memory address register bits	Address bits
PG2 and PG3 -2, -3, -4, and -5	Page register bits	Address bits
S200 through S215 *S200 through *S215	Send data bits	Data bits from processor A register

inverter F8. The disable signal inhibits the write and read operations of all associated micro-memory boards.

When the ENU16 and ENL16 outputs of the output selection detectors F10 and G10 (E11 and G11) are high, they inhibit the respective upper and lower selection multiplexers by enabling the high impedance state. When the ENU16 is low, the upper 16 (17) bit memory data, MM00 through MM15, is enabled; and when the ENL16 is low, the lower 16 (17) bit memory data, MM16 through MM31, is enabled. Each 32 (34)-bit memory bank has an upper 16-bit bank that provides signals to the multiplexer A inputs, and a lower 16-bit bank that provides signals to the multiplexer B inputs. When either the upper or lower 32 (34)-bit output (ENU or ENL low, respectively) is enabled, the high or low state of the ENMMU and ENMMU signals select the A and B inputs. An ENMMU low state selects the MM00-A through MM31-A (S2PAR) data bits to be placed on the MM00 through MM31 (MMU-PAR) lines, and an ENMMU high state selects the MM00-B through MM31-B (S2PAR) data bits to be placed on the MM00 through MM31 (MMU-PAR) lines. This 32 (34)-bit word is applied to the transform, control 1, and control 2 logic elements. In a 32-bit word computer, these data bits are also coupled via *MM00 through *MM31 lines to the processor three-state bus under control of the upper and lower read gates.

During any read cycle, the retrieval of data may be interrupted by the XTPAGE0 signals going low. This drives the ENU16 and ENL16 output high to inhibit the output multiplexers. In addition, if the SELGETMAK signal goes low, the ENU16 signal goes high and inhibits output from the upper 32 (34)-bit memory bank but does not affect output from the lower 32 (34)-bit memory bank.

When any associate micro-memory printed-circuit board has been selected, the disable signal applied to AND gate G10 (G11) causes the ENU16 and ENL16 signal to go high. This causes the read output to be disabled.

512-INSTRUCTION MICRO-MEMORY BOARD

The 512-instruction micro-memory board (figure 4-2) stores a total of 512 x 64 data bits in two 32-bit memory banks, upper and lower. Each upper and lower memory bank contains two 16-bit memory banks, also designated upper and lower. Data being stored (written) or retrieved (read) is under control of the write enable, chip enable, and address bit signals. Stored data bits are the complement of the central processing unit A register output and retrieved data is recomplemented by the chip output. Output data is transferred directly from the chip to the transform, control 1, and control 2. The output 32-bit word is composed of 16 bits from the upper 32-bit memory and 16 bits from the lower 32-bit memory.

Selection

The designation switch (C1) is set at the time of installation to the assigned micro-memory page designation of each individual board. (See table 4-2 for switch settings.) The switch code is applied to the B input of the comparator (C2). When the page bit (PG0 through PG3) code applied to the A input equals the B code, the comparator A = B output at pin 6 goes high. This high state enables the memory selector AND gates (H3 and J3) and applies a low input to OR gate K3 to generate a disable low signal that inhibits the associated micro-memory boards.

Write

When all memory enable (write and chip) signals applied to the memory chips of a 16-bit memory bank are low, the memory bank stores (writes) data in the locations designated by the address bits MA0 through MA7. The write enable signals MMWL16 and MMWU16 are connected to the respective lower and upper 32-bit memory banks to enable data storage into the designated 32-bit zone. The signals, which are applied to the chip enables, select the subordinate (upper or lower) 16-bit memory of the 32-bit zone in which the data is to be stored.

Assume that the MMWU16 signal input to the line drivers is active low. This applies a low to all memory chips to select the upper 32-bit memory zone (B4 through B11, C4 through C11, F4 through F11, and G4 through G11) to store the data present on lines S200 through S215. If the SELGETMAK, CONSTANT 1-1, and CONSTANT 1-2 inputs to the line drives are high, the upper 32-bit memory zone is enabled and ready for selection of the subordinate upper or lower 16-bit memory. A low output of AND gate H3 (ENMMURAM-1) or J3 (ENMMLRAM-1) activates the respective upper or lower 16 bits of the upper 32-bit memory zone when the enable micro-memory upper (ENMMU) input is active (high). When the output signal (ENMMLRAM-1) of AND gate J3 is low, the lower 16-bit memory storage area of the upper 32-bit memory stores the data in chips C4 through C11 at the locations specified by the address bits. If the output signal (ENMMURAM-1) of AND gate H3 is low, the upper 16-bit memory storage area of the upper 32-bit memory stores the data in chips B4 through B11 at locations specified by the address bits.

Storage of the *S200 through *S215 data in the lower 32-bit memory banks (D4 through D11, H4 through H11 for the upper 16; E4 through E11, J4 through J11 for the lower 16) is accomplished in the same manner as described for storage in the upper 32-bit memory, as described in the preceding paragraph. Exceptions to the preceding description include signals CONENABLE 1 and CONENABLE 2 that replace SELGETMAK 1 and 2, and CONSTANT 1-3 and 1-4 that replace CONSTANT 1-1 and 1-2, respectively.

Read

Retrieval (read) of data is enabled when the memory chip write enable is high and all other chip enables are low. This permits the data residing in the addressed location to be placed on the memory output lines for coupling to the transform, control 1, and control 2 logic elements. In systems that employ a 32-bit word, the auxiliary memory outputs (*MM00 through *MM31) are coupled to the central processing unit three-state bus by enabling the upper and lower read gates.

When the MMWU16 signal is high, the read state of the upper 32-bit memory is enabled. If SELGETMAK, CONSTANT 1-1, and CONSTANT 1-2 are all high, the upper 32-bit memory bank is enabled. When the ENMMURAM-1 signal at AND gate H3 goes low, the addressed data bits from the upper 16-bit memory are placed on the MM00 through MM15 lines. These data bits are directly coupled to the transform, control 1, and control 2. If the ENMMLRAM-1 signal at AND gate J3 is low instead of ENMMURAM-1, the lower 16-bit memory is activated. This causes the addressed lower 16 bits to be placed on the MM00 through MM15 lines. If the SELGETMAK, CONSTANT 1-1, or CONSTANT 1-2 signals go low at any time, the read output is inhibited by driving the chip output to the high impedance state.

The lower 32-bit memory bank retrieval (read) is accomplished in the same manner as retrieval of the upper 32-bit memory, described in the preceding paragraphs. When either the upper or lower 32 bit bank is activated, the data bits residing in the addressed locations are placed on the MM16 through MM31 lines. Also, if any one of the chip enable signals goes high, the output is inhibited.

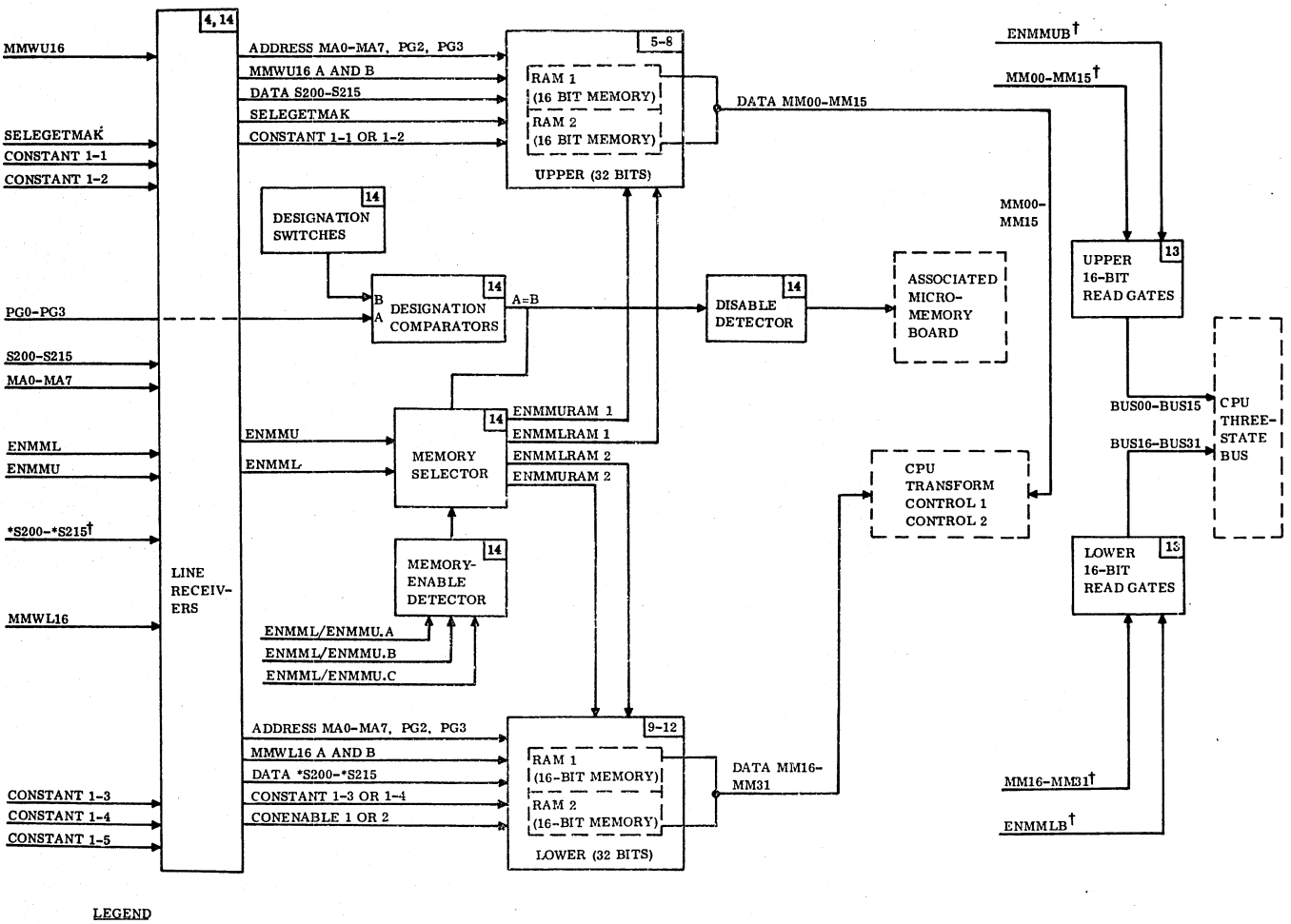
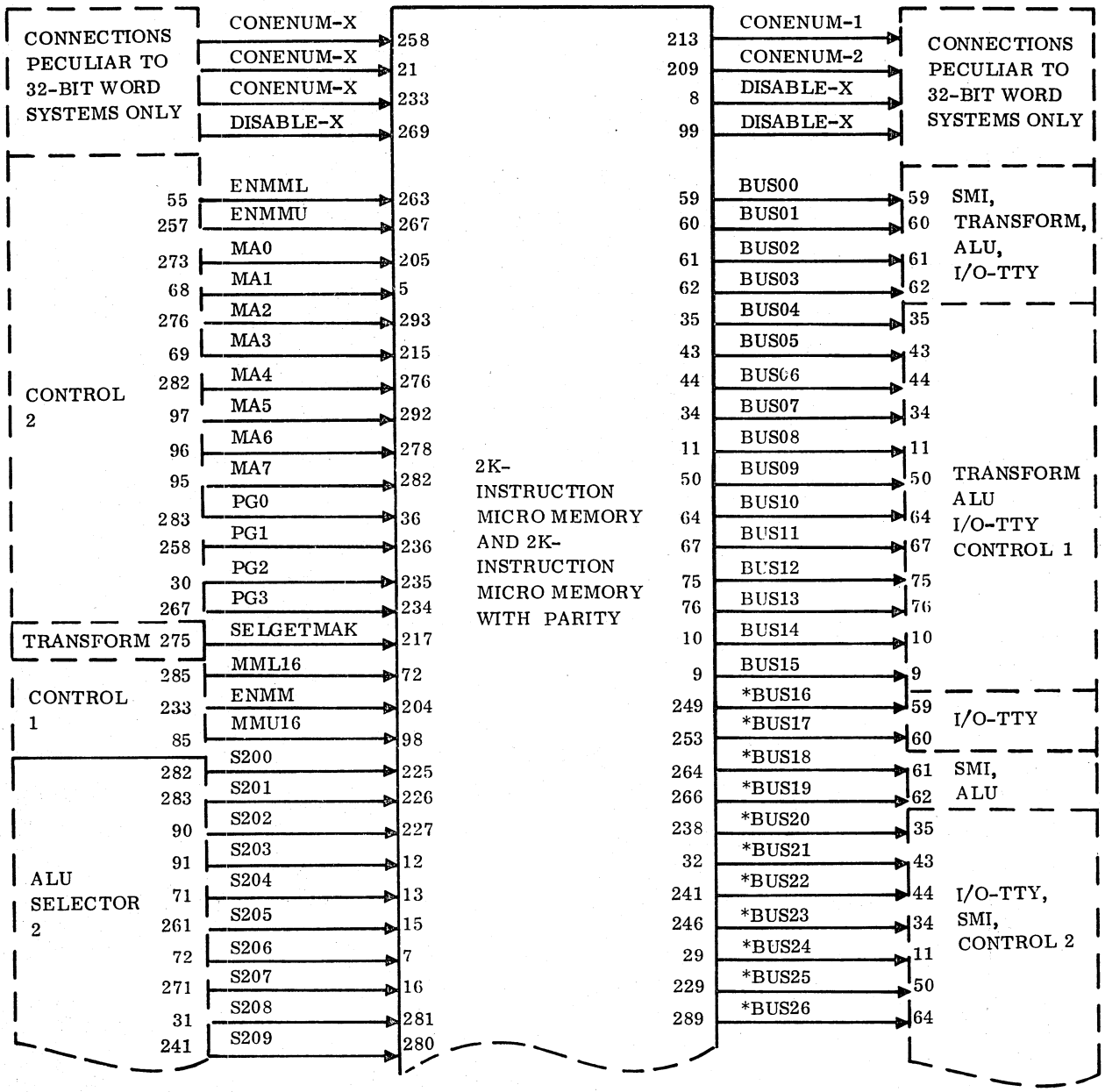


Figure 4-2. 512 Micro Memory Functional Block Diagram

Figures 5-1 and 5-2 present the external input and output signals for the micro memories. Figure 5-1 indicates the external connections for the 2K-instruction micro memory and the 2K-instruction micro memory with parity. Figure 5-2 indicates the external connections for the 512-instruction micro memory.

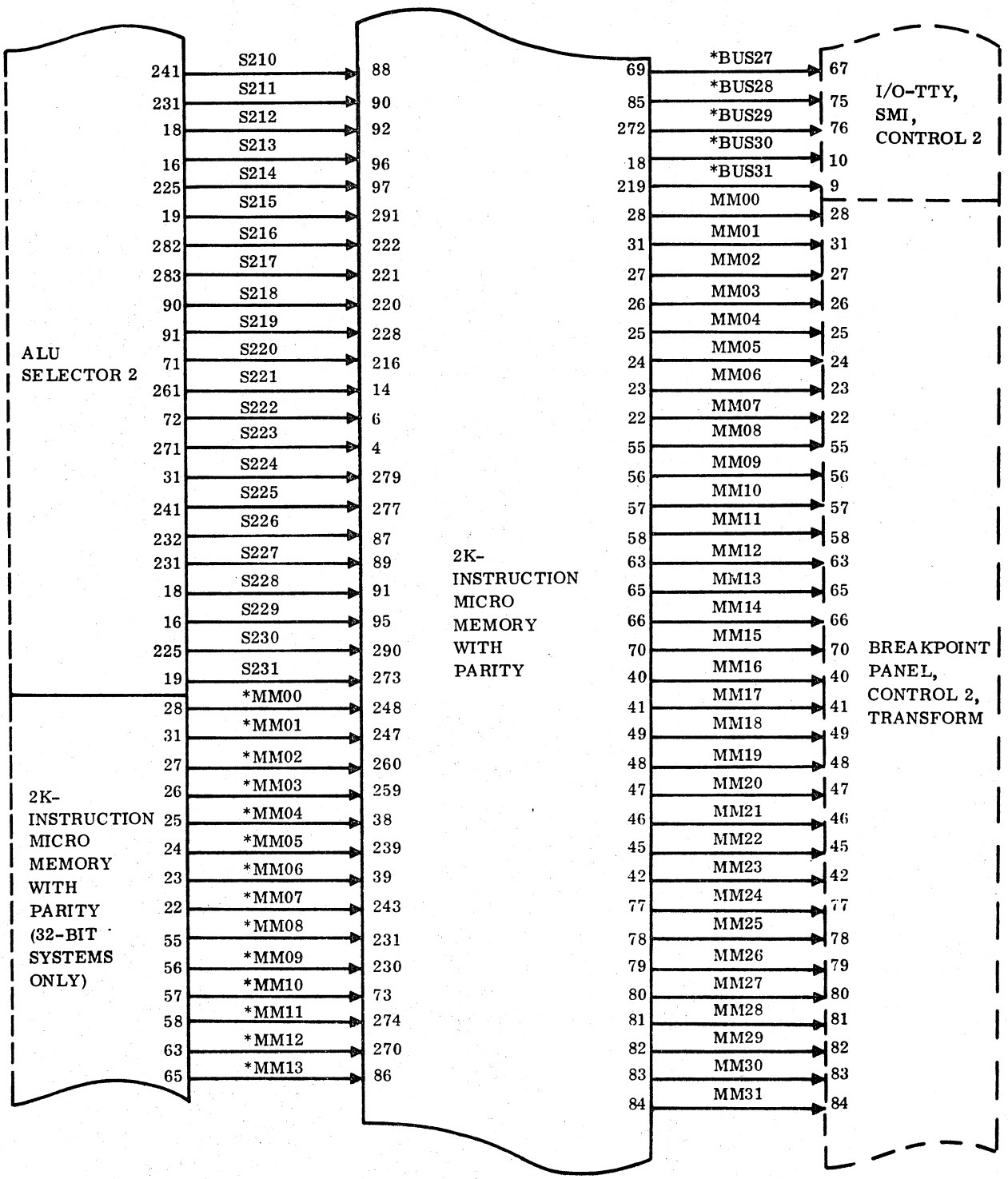
Logic diagrams for the micro memory are contained in the field print package for the appropriate board.



NOTE: ALL SIGNALS WITH ASTERISKS (*) ARE APPLICABLE TO 32-BIT DATA CONFIGURATION SYSTEMS.

0262

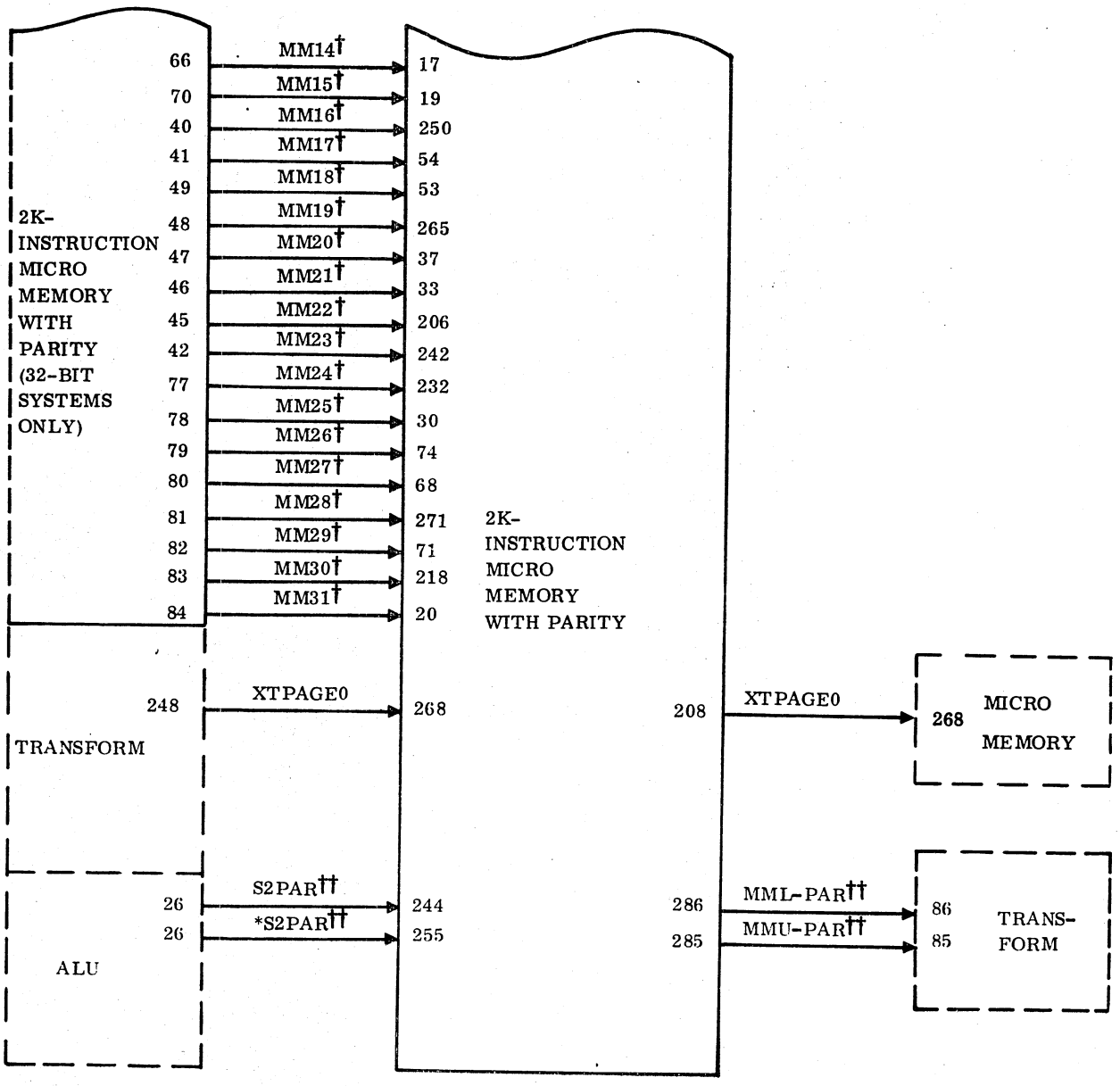
Figure 5-1. 2K-Instruction Micro Memory and 2K-Instruction Micro Memory With Parity External Input and Output Signals (Sheet 1 of 3)



NOTE: ALL SIGNALS WITH ASTERISKS (*) ARE APPLICABLE TO 32-BIT DATA CONFIGURATION SYSTEMS.

0263

Figure 5-1. 2K-Instruction Micro Memory and 2K-Instruction Micro Memory With Parity External Input and Output Signals (Sheet 2 of 3)

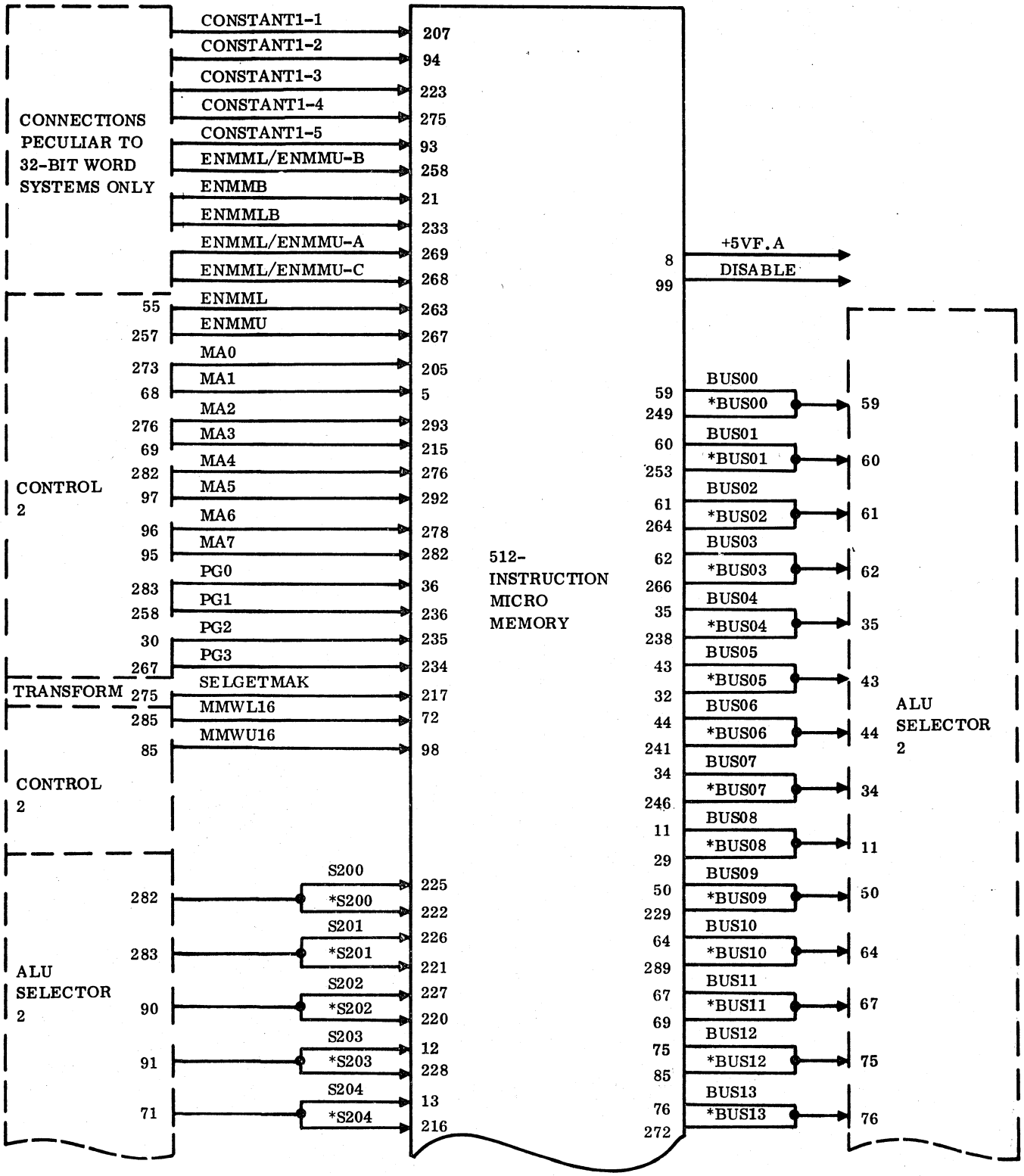


†APPLICABLE TO 32-BIT DATA CONFIGURATION SYSTEMS

††APPLICABLE TO 2K-INSTRUCTION MICRO MEMORY WITH PARITY ONLY

0264

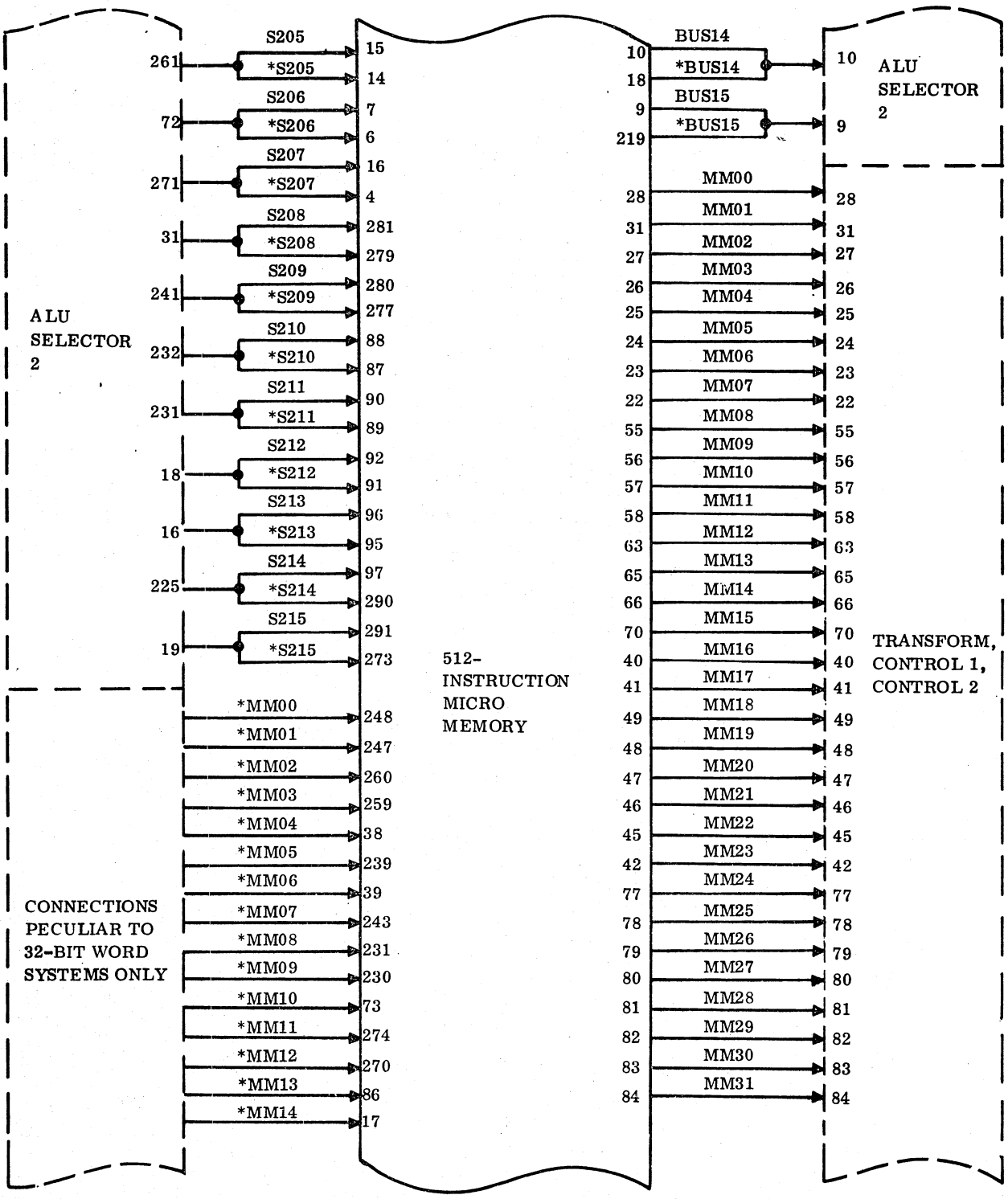
Figure 5-1. 2K-Instruction Micro Memory and 2K-Instruction Micro Memory With Parity External Input and Output Signals (Sheet 3 of 3)



NOTE: ALL SIGNALS WITH ASTERISKS (*) ARE APPLICABLE TO 32-BIT DATA CONFIGURATION SYSTEMS.

0265

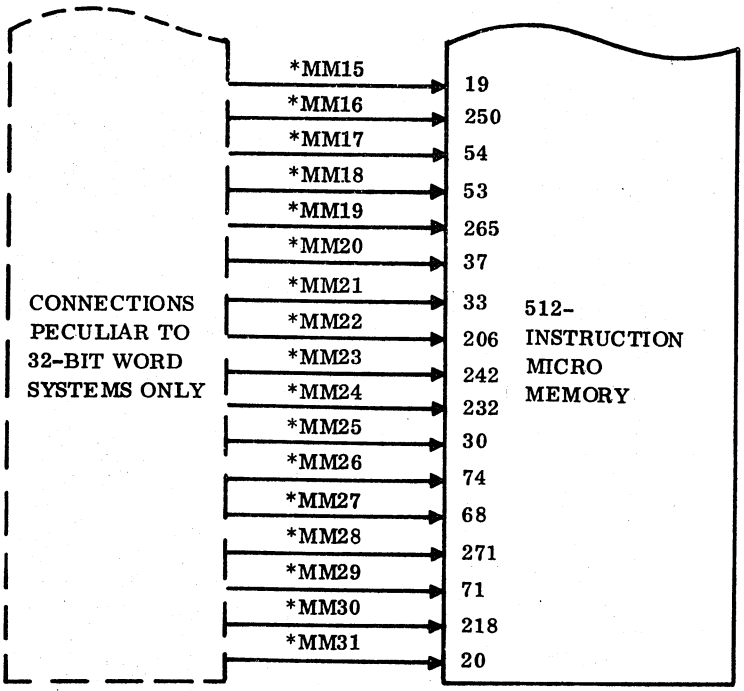
Figure 5-2. 512-Instruction Micro Memory External Input and Output Signals (Sheet 1 of 3)



NOTE: ALL SIGNALS WITH ASTERISKS (*) ARE APPLICABLE TO 32-BIT DATA CONFIGURATION SYSTEMS.

0266

Figure 5-2. 512-Instruction Micro Memory External Input and Output Signals (Sheet 2 of 3)



NOTE: ALL SIGNALS WITH ASTERISKS (*) ARE APPLICABLE TO 32-BIT DATA CONFIGURATION SYSTEMS.

0267

Figure 5-2. 512-Instruction Micro Memory External Input and Output Signals (Sheet 3 of 3)

PREVENTIVE MAINTENANCE

This equipment consists of printed circuit boards that plug into the processor chassis. All preventive maintenance for the memory is covered by the preventive maintenance procedure in the system-level hardware maintenance manual. This consists of cleaning dirt and dust from the boards while performing preventive maintenance on the processor. No additional preventive maintenance is required.

CALIBRATION AND ALIGNMENT

No field calibration and alignment procedures are required.

TROUBLESHOOTING

Troubleshoot to the board level using the MSMP17 and ODS diagnostic memory tests.

Parts data can be obtained in the field print packages listed in the preface.

COMMENT SHEET

MANUAL TITLE CONTROL DATA® 512- and 2048-Instruction Micro Memory

Hardware Maintenance Manual

PUBLICATION NO. 96767900 **REVISION** A

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